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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/807,500	06/11/2001	Rakesh Malik	851663.422USPC	9419

7590 12/01/2004

Seed Intellectual Property Law Group
Suite 6300
701 Fifth Avenue
Seattle, WA 98104-7092

EXAMINER

DO, CHAT C

ART UNIT

PAPER NUMBER

2124

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/807,500	MALIK ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 26 August 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 2-5,7-12 and 18 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 2-5,7-12 and 18 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 8/26/04 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/26/2004.
2. Claims 2-5, 7-12, and 18 are pending in this application. Claims 7-8 and 18 are independent claims. In Amendment, claims 2-5 and 7-12 are amended; claims 1, 6, and 13-17 are cancelled; and claim 18 is added. This action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “the same delay element is used for multiplication by a factor of two and also for a carry function” in every independent claims 7-8 and 18 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 18 is objected to because of the following informalities:

The applicant is advised to change the phrase "+k)*Sn" in line 8 as "k0*Sn" for clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 2-5, 7-12, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 7, the limitation "the same delay element is used for multiplication by a factor of two and also for a carry function" is mis-descriptive because function of the delay element is to delay an input signal by specific amount of predetermined time, but the delay element would not be used or utilized for multiplication by a factor of two. For

examination purposes, the examiner disregards this limitation. Claims 8 and 18 have the same rejection.

Thus, claims 2-5 9-12 are also rejected for being dependent on the rejected based claims 8 and 18 respectively.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Saramaki et al. (U.S. 6,370,556).

Re claim 7, Saramaki et al. disclose in Figure 4 a serial bit FIR filter (abstract) device including: a logic block (51) that receives an $(m+1)$ bit input and produces a transfer function output (y) corresponding to the m th bit position, the logic block including: a combinational-sequential logic block that receives a filter transfer function coefficients (52 and col. 3 lines 54-58) or a predetermined transfer function, the combinational-sequential logic block including $m+1$ combinational logic blocks (53-56 except 55 wherein $m = 3$); and a sequential logic block having m delay element (58-60) for receiving respective outputs of the combinational logic blocks and for providing delayed outputs to respective inputs of the combinational logic blocks respectively;

wherein each combinational logic block B_x includes a plurality of serial subtractor or adder elements (col. 3 lines 58-61), up to a maximum of n , for providing a coefficient multiplication function for each the combinational logic block B_x ; wherein the combinational logic block B_m (53 and 63) output transfer function output according to filter transfer function based on $(m+1)$ -bit input (y) ; and wherein each sequential subtractor or adder element (e.g. 53) includes a carry-out pin (output of 53) fed to an input of one of the sequential subtractor or adder elements (output of 53 is input into 54) of a previous one of the combinational logic blocks such that the same delay element (e.g. 60-61) is used for multiplication by factor of two and also for a carry function (e.g. carrying and delaying a signal from 62 to 63).

Re claim 8, it has general limitations cited in claim 7. Thus, claim 8 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 9, Saramaki et al. further disclose in Figure 4 the combinational circuit implements the addition terms of the filter transfer function using the following form: $(a_0 * S_1 + b_0 * S_2 + \dots + k_0 * S_n) \dots (a_m * S_1 + b_m * S_2 + \dots + k_m * S_n)$ (col. 1 equation 1) where $S_1 \dots S_n$ are input bits and $a_0 \dots a_m$, $b_0 \dots b_m$, $k_0 \dots k_m$, each has a value of $+/ - 1$ or 0 (col. 1 lines 22-27).

Re claim 10, Saramaki et al. further disclose in Figure 4 the coefficient circuit receives n serial input bits (52).

Re claim 11, Saramaki et al. further disclose in Figure 4 the combinational circuit and the sequential circuit are interconnected to implement a finite input response (FIR) filter (abstract).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being obvious over Saramaki et al. (U.S. 6,370,556).

Re claim 12, Saramaki et al. do not disclose the combinational circuit and the sequential circuit are interconnected to implement an infinite input response (IIR) filter. However, the examiner takes an official notice that the concept of IIR filter is well known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to implement an IIR filter into Saramaki et al.'s invention using the method of the same because it would enable to reduce the number of coefficients/order and increase the performance time.

Allowable Subject Matter

11. Claim 18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

12. Claims 2-5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

13. Applicant's arguments filed 08/26/2004 have been fully considered but they are not persuasive.

a. The applicant argues in page 12 for claims 7-12 that Saramaki does not teach or suggest the claimed arrangement in which each subtractor or adder element includes a carry-out pint that is fed to an input of one of the sequential subtractor or adder elements of a previous one of the combination logic blocks.

The examiner respectfully submits that the Saramaki clearly discloses in the claimed invention in Figure 4 as cited in the rejection above wherein each sequential subtractor or adder element (e.g. 53) includes a carry-out pin (output of 53) fed to an input of one of the sequential subtractor or adder elements (output of 53 is input into 54) of a previous one of the combinational logic blocks such that the same delay element (e.g. 60-61) is used for multiplication by factor of two and also for a carry function (e.g. carrying and delaying a signal from 62 to 63).

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

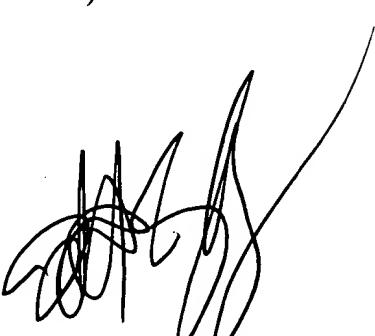
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

November 26, 2004



TODD INBERG
PRIMARY EXAMINER